Amendments to the Claims

1. (CURRENTLY AMENDED) A data processing apparatus, comprising

- a first and second data processing circuit ~~(10a,b)~~, each with an output for outputting memory access requests, at least the first data processing circuit ~~(10a)~~ outputting respective access requests each during a respective validity duration interval;
- a multiplexing circuit ~~(14)~~ with inputs coupled to the outputs of the first and second data processing circuits ~~(10a,b)~~;
- a memory circuit ~~(16, 18)~~ with an input for accepting the access requests successively from an output of the multiplexing circuit ~~(14)~~, each at least after a minimum memory repetition period following acceptance of a preceding access request;
- a timing circuit ~~(11a,b, 12, 15)~~ coupled to the first and second data processing circuit ~~(10a,b)~~ and the memory circuit ~~(16, 18)~~, and arranged to time operation of the first and second processing circuit ~~(10a,b)~~ each substantially periodically, so that the validity duration intervals are substantially periodical with a longer period than the minimum memory repetition period, the timing circuit ~~(11a,b, 12, 15)~~ being arranged to select acceptance time points at which each particular access request from the first data processing circuit ~~(10a)~~ is accepted within the validity duration interval in which this particular access request is made, the timing circuit ~~(11a,b, 12, 15)~~ varying a position of the acceptance time points within the validity duration intervals, so that the position is delayed within the validity duration interval to make room for previously accepting an access request passed by the multiplexing circuit from the second data processing circuit ~~(10b)~~ and the position is moved toward a start of the validity duration interval in successive steps during application of successive access requests from the first data processing circuit within subsequent periods of validity.

2. (CURRENTLY AMENDED) A data processing circuit according to Claim 1, wherein the timing circuit comprises first and second clocking circuits ~~(11a,b)~~ coupled to clock inputs of the first and second data processing circuit ~~(10a,b)~~ respectively, whereby the access requests, if made, are replaced by the first and

second data processing circuit ~~(10a,b)~~ at a first and second frequency of the first and second clocking circuit ~~(11a,b)~~ respectively, the sum of the first and second frequency being smaller than the inverse of the minimum memory repetition period.

3. (CURRENTLY AMENDED) A data processing circuit according to Claim 2, wherein the timing circuit comprises an asynchronous arbiter circuit ~~(40)~~ with inputs coupled to the first and second clocking circuit ~~(11,ab)~~ and an output coupled to a control input of the multiplexing circuit ~~(14)~~, the arbiter circuit ~~(40)~~ being arranged to control from which of the first and second data processing circuit ~~(10a,b)~~ the multiplexing circuit ~~(14)~~ will pass the access request, the arbiter circuit ~~(40)~~ selecting among the data processing circuits ~~(10a,b)~~ on a first come first served basis of transitions in clock signals of the first and second data processing circuit ~~(10a,b)~~.

4. (CURRENTLY AMENDED) A data processing circuit according to Claim 3, comprising an asynchronous timer circuit ~~(15)~~ with a trigger input coupled to asynchronous arbiter circuit ~~(40)~~ and arranged to generate a timing signal for accessing the memory ~~(18)~~, the asynchronous timer circuit ~~(40)~~ triggering a memory access cycle each time when asynchronous arbiter circuit ~~(40)~~ selects a request and a previous minimum memory repetition period has finished.

5. (CURRENTLY AMENDED) A data processing circuit according to Claim 1, the memory circuit comprising a register ~~(16)~~ and a storage unit ~~(18)~~, the register ~~(16)~~ coupled between the first data processing circuit ~~(10a)~~ and the storage unit ~~(18)~~, for latching access request information from at least the first data processing circuit ~~(10a)~~ for use by the storage unit ~~(18)~~ under control of the timing circuit ~~(11a,b, 12, 15)~~, upon the delay determined by the timing circuit ~~(11a,b, 12, 15)~~.

6. (CURRENTLY AMENDED) A data processing circuit according to Claim 1, wherein the memory circuit ~~(12, 18)~~ comprises a series of successively coupled pipeline stages ~~(50a-d)~~, for executing successive steps in response to an access request, the minimum memory repetition period corresponding to a time interval needed by one of the pipeline stages to execute one of the steps.

7. (CURRENTLY AMENDED) A data processing circuit according to Claim 6, wherein the memory circuit ~~(16, 18)~~ comprises memory banks ~~(52a-d)~~, each coupled to a respective one of the pipe-line stages ~~(50a-d)~~, for processing each of the requests successively in different ones of the banks ~~(52a-d)~~.

8. (CURRENTLY AMENDED) A data processing circuit according to Claim 7, wherein the banks ~~(52a-d)~~ are arranged at successive positions along a spatial row on an integrated circuit, with read data outputs for outputting data read in response to read requests among the requests at successive positions along the row, the second data processing circuit ~~(10b)~~ comprising display driver circuits, coupled to the outputs.

9. (CURRENTLY AMENDED) A data processing circuit according to Claim 1, comprising a data register ~~(19)~~ coupled between the memory circuit ~~(16, 18)~~ and the second data processing circuit ~~(10b)~~, for copying read data read from the memory circuit ~~(10a,b)~~ in response to read requests among the requests and for supplying the read data to the second data processing circuit ~~(10b)~~ during handling of access requests of the first data processing circuit ~~(10a)~~.

10. (CURRENTLY AMENDED) A data processing circuit according to Claim 9, wherein the memory circuit ~~(12, 16)~~ comprises a plurality of banks ~~(52a-d)~~ with a first data word length, write requests among the requests comprising bank selection information and write data of the first data word length, the data register ~~(18)~~ having a second data word length for receiving data from a plurality of the banks ~~(52a-d)~~ in parallel in response to each read request.

11. (CURRENTLY AMENDED) A data processing circuit according to Claim 1, wherein the second data processing circuit ~~(10b)~~ comprises display drivers for processing read data from the memory by driving a content of a display device dependent on the read data.

12. (CURRENTLY AMENDED) A method of processing data the method comprising

- providing a memory circuit ~~(16, 18)~~ capable of accepting successive access requests each time after a minimum memory repetition period;
- generating access request signals at a first and second output of a plurality of data processing circuits ~~(10a,b)~~, access requests remaining each time for a validity duration interval at the first output, the validity duration interval being larger than the minimum memory repetition period;
- time-multiplexing access requests from the first and second output to the memory circuit ~~(12, 16)~~;
- controlling a delay between the start of the validity duration intervals in which the first output outputs the access requests and acceptance of the access requests from the periods of validity, the delay being reduced in successive steps during application of successive access requests from the first output, until the delay in a particular period of validity lies at least one minimum memory repetition period before the end of the particular period of validity;
- subsequently causing acceptance of at least one of the access requests from the second output, increasing the delay before a next access request of the first data processing circuit is accepted within the period of validity in which this next access request remains at the output.